



112

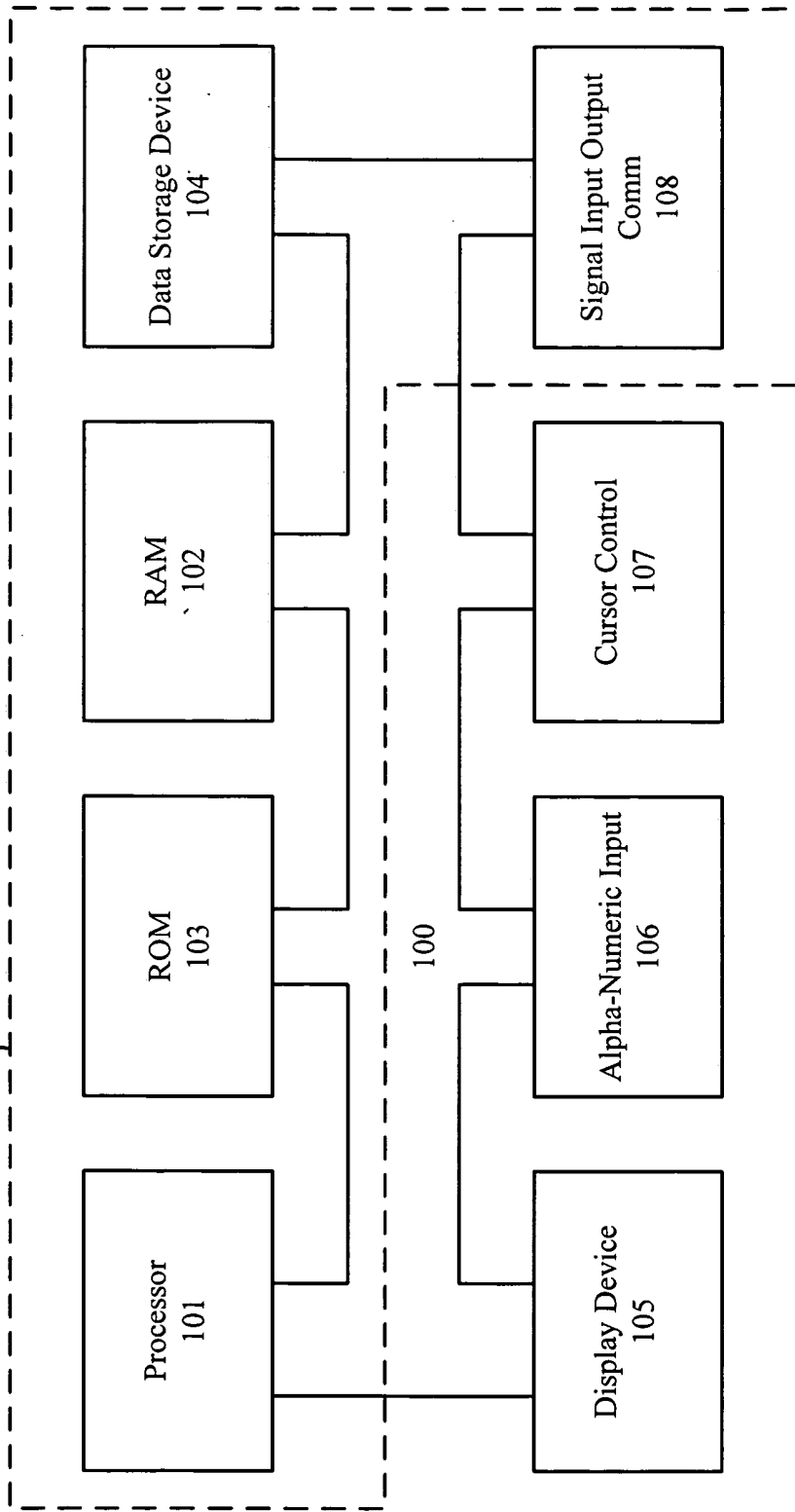


Figure 1

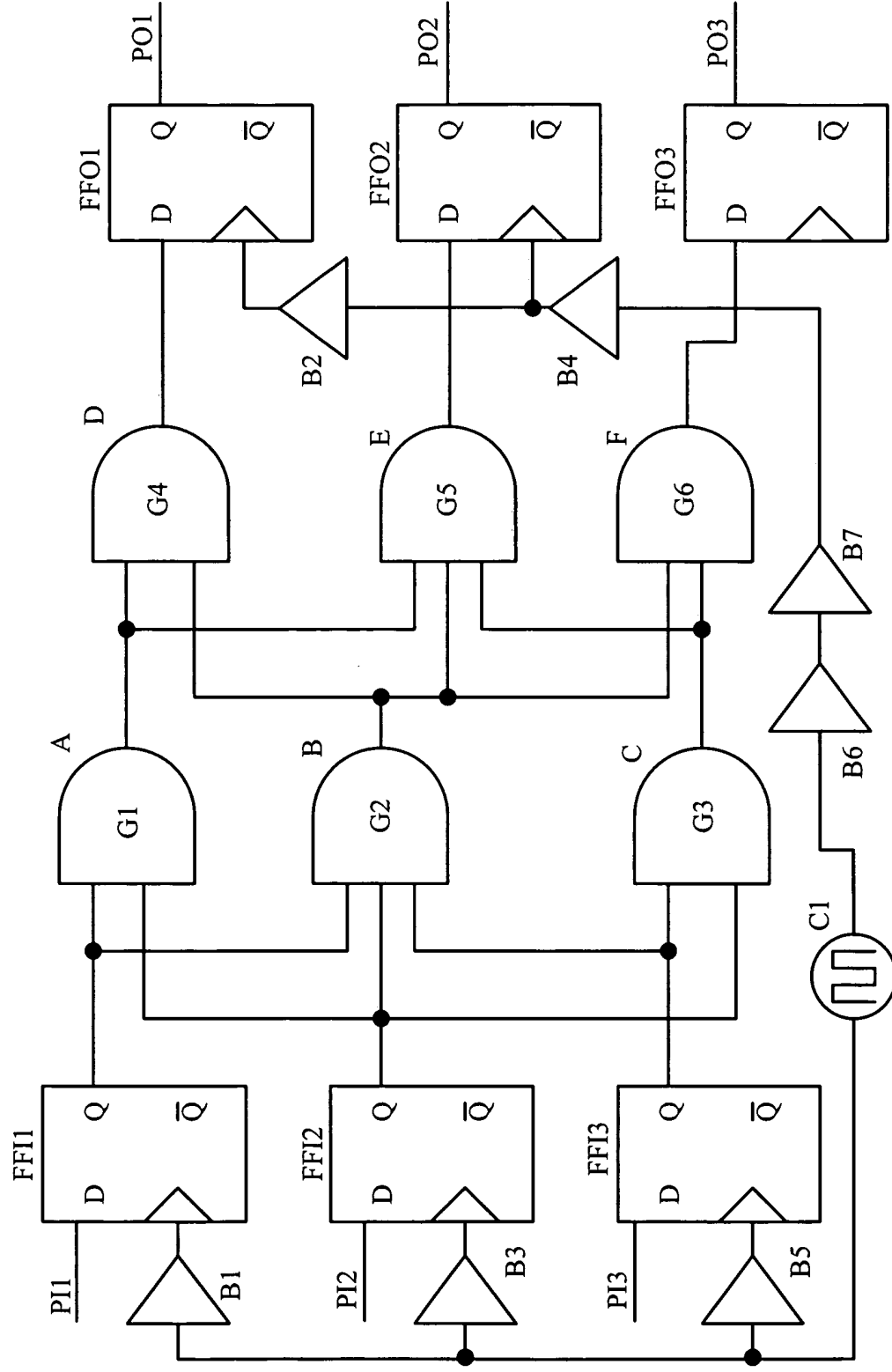


Figure 2A

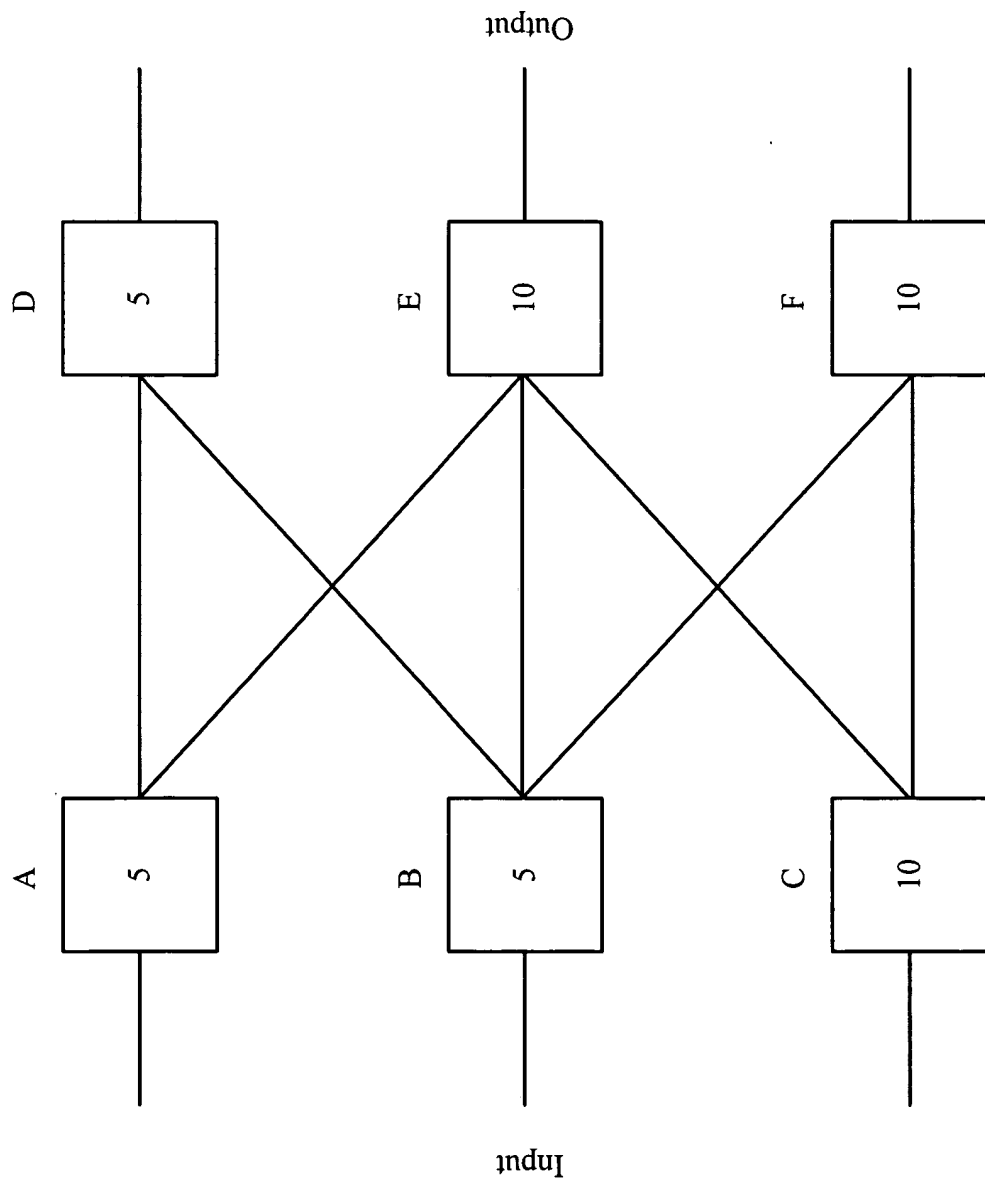


Figure 2B

Forward Delay Sums

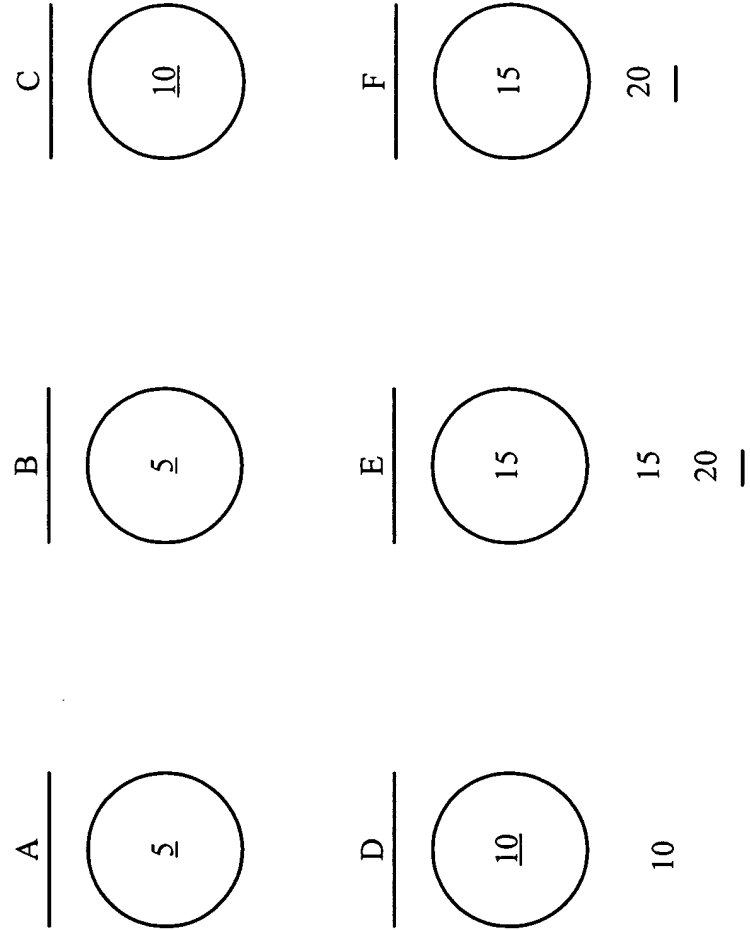


Figure 3

T_{qi}	T_{sj}	T_{hj}	Hold Time Constraint	Minimum Forward Delay Sum	Maximum Forward Delay Sum	Setup Time Constraint	Output Node
2	12	9	7	10	10	26	D
2	3	8	6	15	20	35	E
2	19	10	8	15	20	19	F

Clock Period = 40

Setup Time Constraint = Clock Period – T_{qi} - T_{sj}

Hold Time Constraint = T_{hj} - T_{qi}

Figure 4

Reverse Delay Differences

<u>D</u>	<u>E</u>	<u>F</u>
<u>21</u>	<u>25</u>	9
<u>A</u>	<u>B</u>	<u>C</u>
<u>16</u>	16	15
20	20	-1
	4	<u> </u>

Figure 5

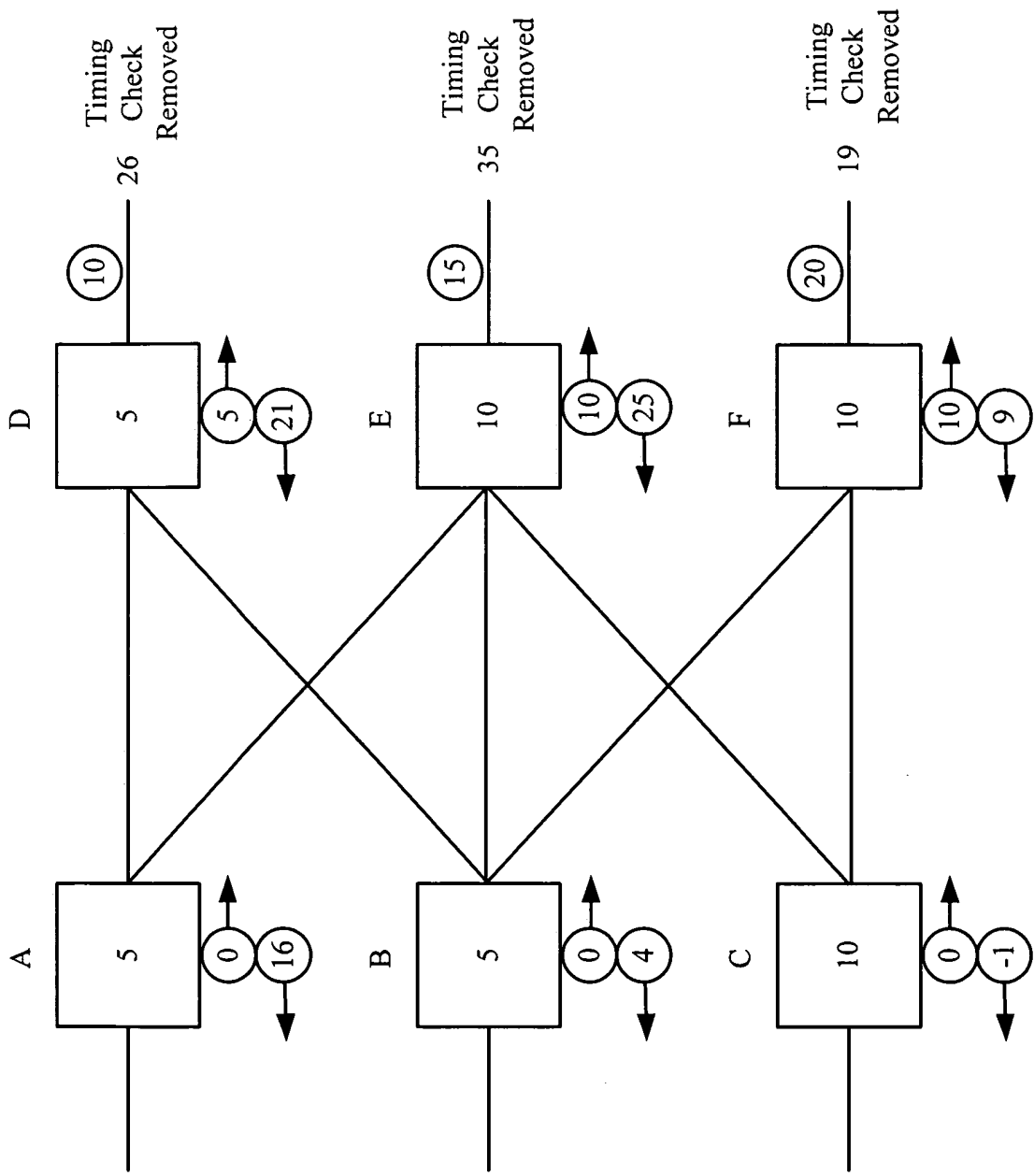


Figure 6

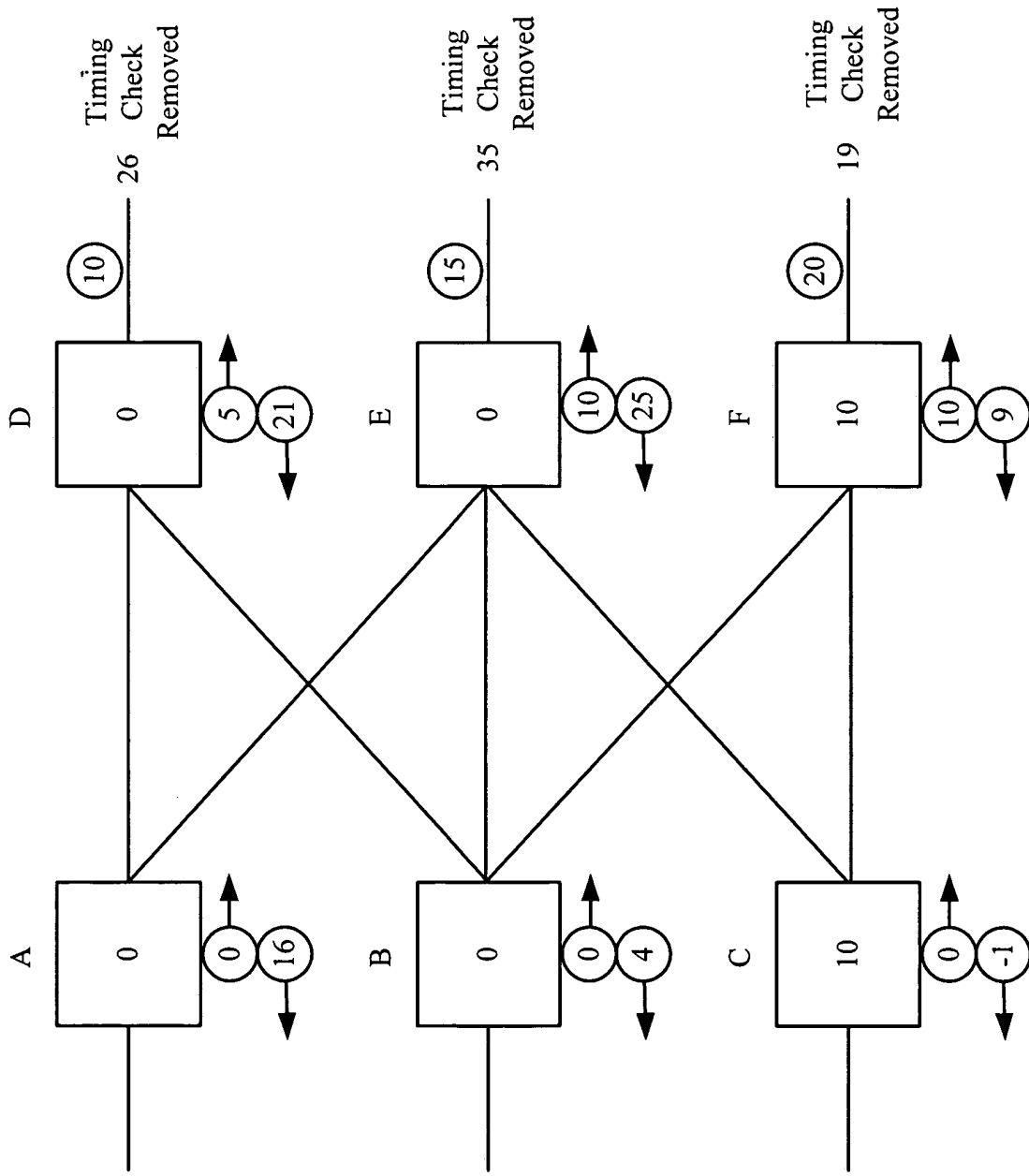


Figure 7A

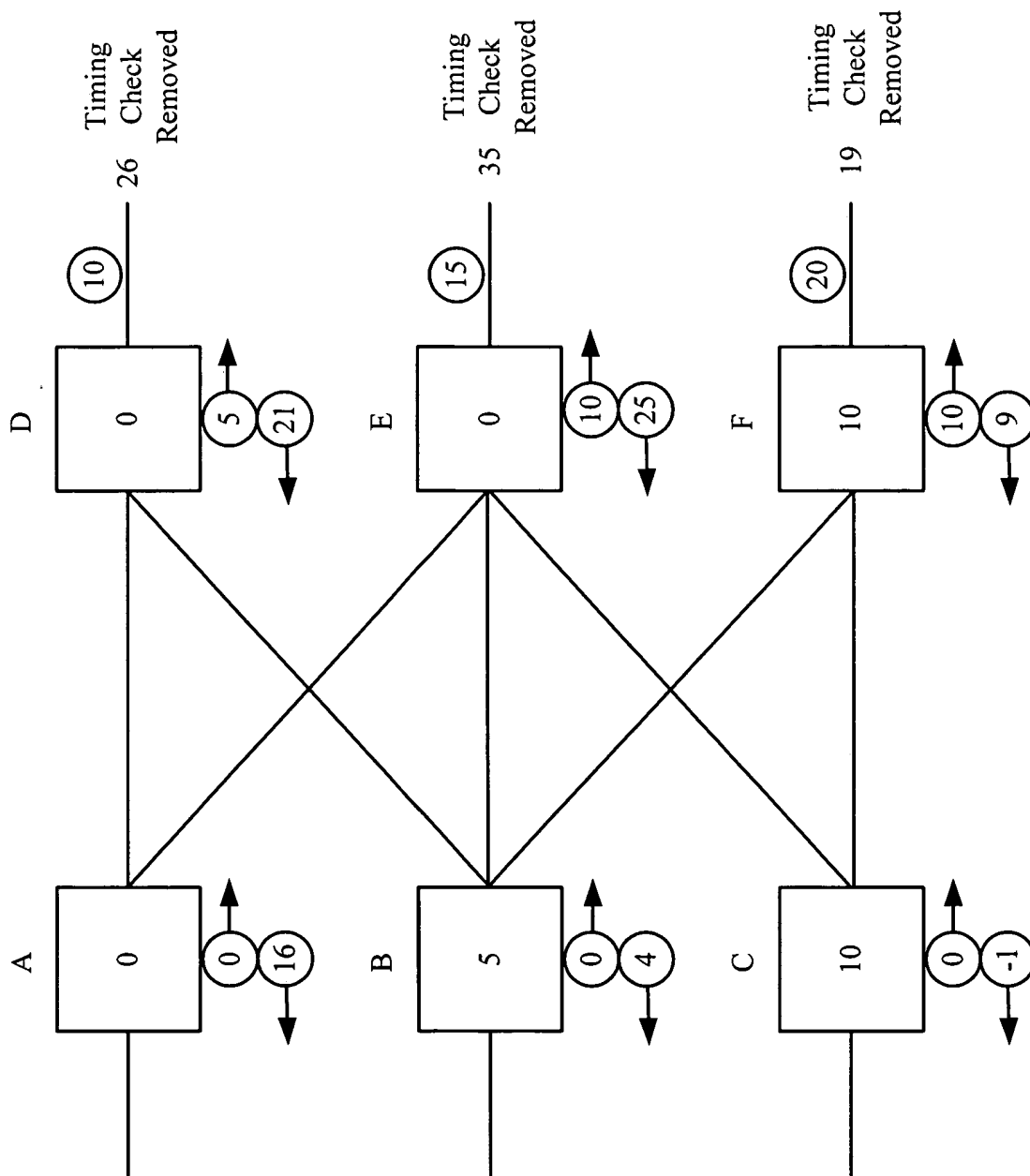


Figure 7B

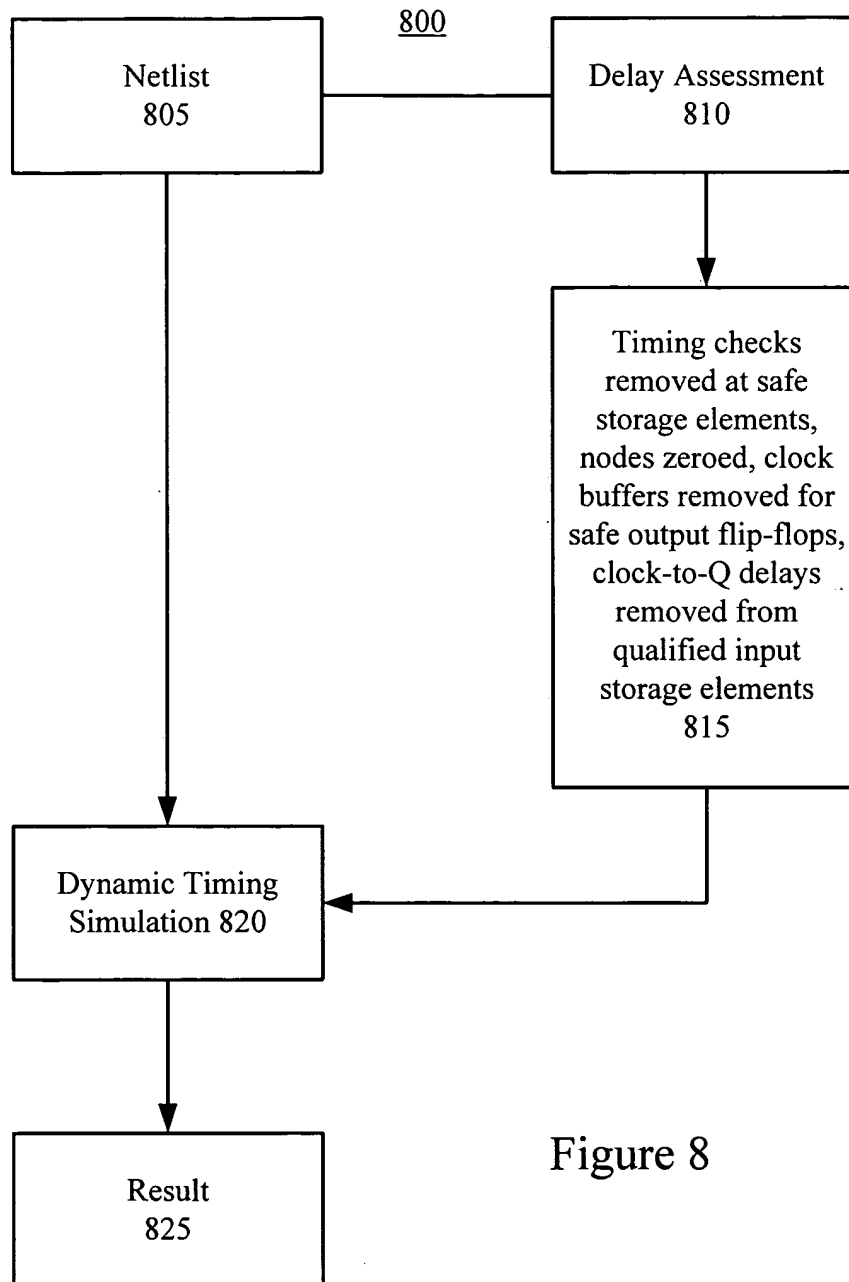


Figure 8

900

905

Access combinational portion of
circuit for analysis

910

Determine maximum forward
delay sums

915

Determine safe output nodes
based upon safe delay period

920

Remove timing checks and clock
buffer delays from safe storage
elements

925

Determine minimum reverse
delay differences

930

Set forward delay to zero for
nodes having a reverse delay
difference greater than the
maximum forward delay sum,
remove clock-to-Q delays from
qualified input storage element

935

Perform dynamic simulation on
the netlist for circuits that have
timing checks removed, use a
zero delay model, e.g. cycle based
simulation is performed with
respect to this logic to enhance
the speed of dynamic simulation

Figure 9

Delay
Assessment